COURSE PLAN

FIRST: BASIC INFORMATION

College	
College	: Karak College
Department	: Engineering Department

Course	
Course Title	: Digital System Design
Course Code	: 020406221
Credit Hours	: 3 (1 Theoretical, 2 Practical)
Prerequisite	: 020406132 / 020406121

Instructor					
Name	:				
Office No.	:				
Tel (Ext)	:				
E-mail	:				
Office Hours	:				
Class Times	Building	Day	Start Time	End Time	Room No.

Text Book

1. Digital System design, Al-Balqa Applied University & KOICA, 2022

References

1. Brock J. LaMeres, “Introduction to Logic Circuits & Logic Design with Verilog,” 2nd Edition, Springer, 2019
2. Volnei Pedroni, “Circuit Design with VHDL” 3rd Edition; The MIT Press, 2020.
3. Blaine Readler, “VHDL by Example”, Full Arc Press, 2014.

SECOND: PROFESSIONAL INFORMATION

COURSE DESCRIPTION

This course deals with methods for efficient design of high-performance application-specific integrated circuits, and for this purpose, digital systems and hardware description languages(HDLs) are explained together. It specifically covers how to use Verilog, and how to design, implement, and test commonly used analog and digital circuits using Verilog.

COURSE OBJECTIVES

The objectives of this course are to enable the student to do the following:

- Learn and use modern hardware/software design tools to develop modern digital systems.
- Gain an in-depth understanding of hardware description language(HDL)
- Realize different circuits in sequential and combinational ways
- Explain the applications of VHDL in PLDs(Programmable Logic Device) and FPGAs(Field Programmable Gate Array)

- Explain the synthesis, verification and implementation processes targeting FPGAs.

COURSE LEARNING OUTCOMES

By the end of the course, the students will be able to:

CLO1. Explain the basic concept of digital systems
CLO2. Explain and use the basic components of digital systems
CLO3. Design and analysis combinational logic design
CLO4. Apply Verilog to design combinational logic circuits
CLO5. Design and analysis sequential logic design
CLO6. Apply Verilog to design sequential logic circuits
CLO7. Explain various kinds of programmable hardware

COURSE SYLLABUS

Week	Topic	Topic Details	Reference (Chapter)	Proposed Assignments
1	Review	• Analog v.s. digital • Number systems • Base conversion • Binary arithmetic	CLO1	
2	Digital Circuitry and Interfacing	• Basic gates • Digital circuit operation • Logic families • Driving loads	CLO2	
3	Combinational Logic Design	• Boolean algebra • Combinational logic analysis • Combinational logic synthesis • Logic minimization	CLO3	
4	Verilog - Combinational	• History of hardware description languages • HDL abstraction • Modern digital design flow	CLO4	
5	Verilog - Combinational	• Data types • Module • Operators	CLO4	
6	Verilog - Combinational	• Modeling concurrent functionality in Verilog • Structural design and hierarchy • Overview of simulation test benches	CLO4	
7	Verilog - Combinational	• Decoders • Encoders • Multiplexers • Demultiplexers	CLO4	
8	**Midterm Exam**			
9	Verilog - Combinational	• Adder • Subtractor • Multiplier	CLO4	

Week	Topic	Topic Details	Reference (Chapter)	Proposed Assignments
		• Divider		
10	Sequential Logic Design	• Sequential logic storage devices • Sequential logic timing consideration • Finite state machines(FSMs) • Counters	CLO5	
11	Verilog - Sequential	• Procedural assignment • Conditional programming constructs • System tasks • Test benches	CLO6	
12	Verilog - Sequential	• Modeling sequential storage devices in Verilog • Latches • Flip-flops	CLO6	
13	Verilog - Sequential	• Modeling finite state machines in Verilog • State memory block • Next state logic block • Output logic block	CLO6	
14	Verilog - Sequential	• Serial bit sequence detector • Vending machine controller • Up/Down counter	CLO6	
15	Programmable Logic	• Programmable logic devices • Programmable arrays • Field programmable gate arrays	CLO7	
16	**Final Exam**			

COURSE LEARNING RESOURCES

This module will be taught using available resources including:

- Class lectures, lecture notes, assignments, quizzes, and exams designed to achieve the course objectives.
- Lectures and materials uploaded to the e-learning system.
- Student should read the material covered in class, complete assignments on time, participate in class discussions, and do whatever it takes to grasp the topics.

ONLINE RESOURCES

Any web site or tutorial that offers information about the basics and principles of power electronics analysis.

ASSESSMANT TOOLS

ASSESSMENT TOOLS	%
Projects and Quizzes	20
Mid Exam	30

	Final Exam	50	
	TOTAL MARKS	100	

THIRD: COURSE RULES

ATTENDANCE RULES

Attendance and participation are extremely important, and the usual University rules will apply. Attendance will be recorded for each class. Absence of 10% will result in a first written warning. Absence of 15% of the course will result in a second warning. Absence of 20% or more will result in forfeiting the course and the student will not be permitted to attend the final examination. Should a student encounter any special circumstances (i.e. medical or personal), he/she is encouraged to discuss this with the instructor and written proof will be required to delete any absences from his/her attendance records.

GRADING SYSTEM

The grading system for the Diploma Degrees in the Al-Balqa' Applied University is the total mark out of 100%

GRADE	POINTS
FAILED	0-49
PASSED	50-100

REMARKS

Copying assignments, quizzes, or exams from another student will not be tolerated.
Helping other students to cheat in any way or form will not be tolerated.
Excellent attendance is expected.
BAU policy requires the faculty member to assign 35 grade if a student misses 15% of the classes without a valid excuse.
If student miss a class, it is his responsibility to find out about any announcements or assignments he/she may have missed.
Participation in, and contribution to class discussions will affect the final grade positively.
Making any kind of disruption (side talks or mobile ringing) in the class is not allowed and it will affect student negatively.
Makeup exam should not be given unless there is a valid excuse according to BAU policies.

COURSE COORDINATOR

Course Coordinator:	**Department Head:**
Signature:	**Signature:**
Date:	**Date:**